CLAIMS

What is claimed is:

1. A programmable clock circuit to generate frequencies from an input clock signal having a predetermined frequency and having a rising edge and a falling edge associated with each clock cycle of the input clock signal, the circuit comprising:

a counter configured to receive the input clock signal and to generate a counter signal having a frequency of M cycles for every N cycles of the input clock signal;

a comparator circuit coupled to the counter to compare a count value of the counter with predetermined count values and to generate comparator signals related to the comparison; and

a control circuit to generate an output clock signal based on the comparator signals to thereby select a rising edge of the output clock signal based a rising edge or a falling edge of the input clock signal and to select a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal.

2. The circuit of claim 1 wherein the control circuit generates the output clock signal with a rising edge of the output clock signal based on a rising edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to zero and less than M/2.

3. The circuit of claim 1 wherein the control circuit generates the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to M/2 and less than M.

4. The circuit of claim 1 wherein the counter is a M/N:D counter where D is related to a duty cycle of the output clock signal.

5. The circuit of claim 4 wherein the control circuit generates the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to D and less than D+M/2.

6. The circuit of claim 4 wherein the control circuit generates the output clock signal with a falling edge of the output clock signal based on a falling edge of the input clock signal if the comparator signals indicate that the counter has a value greater than or equal to D+M/2 and less than D+M.

7. The circuit of claim 4 wherein the control circuit generates the output clock signal with 50% duty cycle.

8. The circuit of claim 4 wherein D is programmed with a ½ integer resolution.

9. The circuit of claim 1, further comprising a mode control input to override the control circuit wherein the control circuit generates the output clock signal with a rising edge and a falling edge of the output clock signal based on a rising edge of the input clock signal irrespective of the comparator signals.

10. The circuit of claim 1 wherein the comparator circuit comprises first, second and third comparators, the first comparator comparing the counter value with a value of M and M/2, the second comparator comparing the counter value with a value D, where D is a programmable value related to a duty cycle of the output signal, and the third comparator comparing the counter value with a value of D+M and D+M/2.

11. The circuit of claim 10, further comprising an adder to add a value of minus D to the counter value wherein the second comparator compares the counter value minus D to 0 and the third comparator compares the counter value minus D with a value of M and M/2.

12. The circuit of claim 1 wherein the control circuit comprises first and second synchronization latches wherein the first synchronization latch generates the output signal rising edge based on a rising edge of a selected input clock cycle if activated, the second synchronization latch generates a signal to generate the output signal rising edge based on a falling edge of an input clock cycle preceding the selected input clock cycle if activated.

13. The circuit of claim 1 wherein the control circuit comprises first and second synchronization latches wherein the first synchronization latch generates the output signal falling edge based on a rising edge of a selected input clock cycle if activated, the second synchronization latch generates a signal to generate the output

signal falling edge based on a falling edge of an input clock cycle preceding the selected input clock cycle if activated.

14. A programmable clock circuit comprising:

an input clock signal having a predetermined frequency and having a rising edge and a falling edge associated with each clock cycle of the input clock signal; and

a control circuit to generate an output clock signal having a frequency of M cycles for every N cycles of the input clock signal and to select a rising edge of the output clock signal based a rising edge or a falling edge of the input clock signal and to select a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal.

15. The circuit of claim 14 wherein the control circuit is a state machine that generates selected cycles of the output clock signal with a rising edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock.

16. The circuit of claim 14 wherein the control circuit is a state machine that generates selected cycles of the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a falling edge of the output clock signal based on a falling edge of the input clock.

17. The circuit of claim 14, further comprising a storage area containing data indicating which of the M cycles of the output clock signal having a rising edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having a rising edge based on a falling edge of the input clock, the control circuit using the storage area data to generate the output clock signal.

18. The circuit of claim 14, further comprising a storage area containing data indicating which of the M cycles of the output clock signal having a falling edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having a falling edge based on a falling edge of the input clock, the control circuit using the storage area data to generate the output clock signal.

19. A programmable clock circuit comprising:

means for receiving an input clock signal having a predetermined frequency and having a rising edge and a falling edge associated with each clock cycle of the input clock signal; and

control means for generating an output clock signal having a frequency of M cycles for every N cycles of the input clock signal and for selecting a rising edge of the output clock signal based a rising edge or a falling edge of the input clock signal and for selecting a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal.

20. The circuit of claim 19 wherein the control means comprises counter means for generating a counter value based on the input clock signal and comparison means for comparing the counter value to predetermined count values and output control means for generating the output clock signal with the rising edge of the output clock signal based a rising edge or a falling edge of the input clock signal and a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal based on the comparing by the comparison means.

21. The circuit of claim 20 wherein the control means generates the output clock signal with a rising edge of the output clock signal based on a rising edge of the input clock signal if the comparator means indicates that the counter value is greater than or equal to zero and less than M/2.

22. The circuit of claim 20 wherein the control means generates the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock signal if the comparator means indicates that the counter value is greater than or equal to M/2 and less than M.

23. The circuit of claim 20 wherein the counter means comprises a M/N:D counter where D is related to a duty cycle of the output clock signal.

24. The circuit of claim 23 wherein the control means generates the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock signal if the comparator means indicates that the counter value is greater than or equal to D and less than D+M/2.

25. The circuit of claim 23 wherein the control means generates the output clock signal with a falling edge of the output clock signal based on a falling edge

of the input clock signal if the comparator means indicates that the counter value is greater than or equal to D+M/2 and less than D+M.

26. The circuit of claim 19 wherein the control means comprises a state machine that generates selected cycles of the output clock signal with a rising edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock.

27. The circuit of claim 19 wherein the control means comprises a state machine that generates selected cycles of the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a falling edge of the output clock signal based on a falling edge of the input clock.

28. The circuit of claim 19, further comprising storage means for storing data indicating which of the M cycles of the output clock signal having a rising edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having a rising edge based on a falling edge of the input clock, the control means using the stored data to generate the output clock signal.

29. The circuit of claim 19, further comprising storage means for storing data indicating which of the M cycles of the output clock signal having a falling edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having a falling edge based on a falling edge of the input clock, the control means using the stored data to generate the output clock signal.

30. The circuit of claim 19, further comprising mode control means for overriding the control means wherein the control means always generates the output clock signal with a rising edge and a falling edge of the output clock signal based on a rising edge of the input clock signal.

31. A method for generating programmable clock frequencies comprising:

receiving an input clock signal having a predetermined frequency and having a rising edge and a falling edge associated with each clock cycle of the input clock signal; and

generating an output clock signal having a frequency of M cycles for every N cycles of the input clock signal with a rising edge of the output clock signal based a rising edge or a falling edge of the input clock signal and a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal.

32. The method of claim 31 wherein generating the output clock signal comprises:

generating a counter value based on the input clock signal;

comparing the counter value to predetermined count values; and

generating the output clock signal with the rising edge of the output clock signal based a rising edge or a falling edge of the input clock signal and with a falling edge of the output clock signal based on a rising edge or a falling edge of the input clock signal based on the comparing.

33. The method of claim 32 wherein the output clock signal is generated with a rising edge of the output clock signal based on a rising edge of the input clock signal if the comparing indicates that the counter value is greater than or equal to zero and less than M/2.

34. The method of claim 32 wherein the output clock signal is generated with a rising edge of the output clock signal based on a falling edge of the input clock signal if the comparing indicates that the counter value is greater than or equal to M/2 and less than M.

35. The method of claim 32 wherein the counting uses a M/N:D counter where D is related to a duty cycle of the output clock signal.

36. The method of claim 35 wherein the output clock signal is generated with a falling edge of the output clock signal based on a rising edge of the input clock signal if the comparing indicates that the counter value is greater than or equal to D and less than D+M/2.

37. The method of claim 35 wherein the output clock signal is generated with a falling edge of the output clock signal based on a falling edge of the input clock signal if the comparing indicates that the counter value is greater than or equal to D+M/2 and less than D+M.

38. The method of claim 31 wherein generating the output clock signal comprises using a state machine that generates selected cycles of the output clock signal with a rising edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a rising edge of the output clock signal based on a falling edge of the input clock.

39. The method of claim 31 wherein generating the output clock signal comprises using a state machine that generates selected cycles of the output clock signal with a falling edge of the output clock signal based on a rising edge of the input clock and selected cycles of the output clock signal with a falling edge of the output clock signal based on a falling edge of the input clock.

40. The method of claim 31, further comprising storing data indicating which of the M cycles of the output clock signal having a rising edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having a rising edge based on a falling edge of the input clock, the generating the output clock signal using the stored data to generate the output clock signal.41. The method of claim 31, further comprising storing data indicating which of the M cycles of the output clock signal having a falling edge based on a rising edge of the input clock and which of the M cycles of the output clock signal having a falling edge based on a falling edge of the input clock, the generating the output clock signal using the stored data to generate the output clock signal.

42. The method of claim 31, further comprising generating a mode control signal to override the generating the output clock signal wherein generating the output clock signal always generates the output clock signal with a rising edge and a falling edge of the output clock signal based on a rising edge of the input clock signal.